EE 330
Lecture 36

Digital Circuit Design

- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter

Exam Schedule

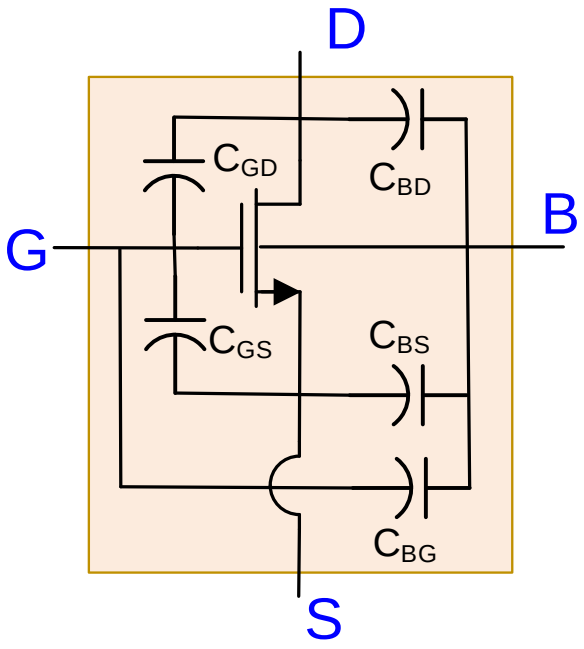
Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review from Last Lecture

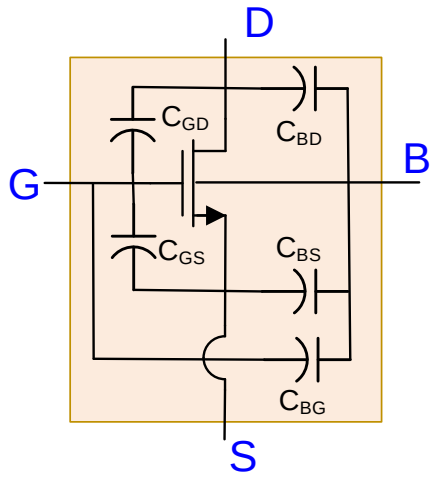
Parasitic Capacitance Summary



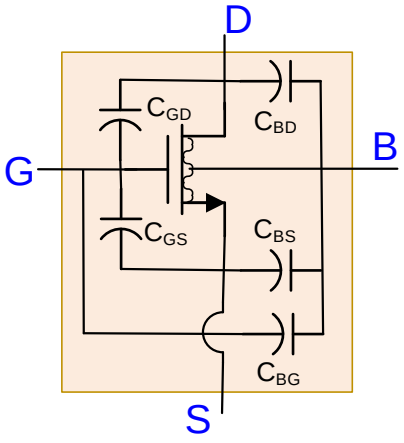
	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Review from Last Lecture

Parasitic Capacitance Summary

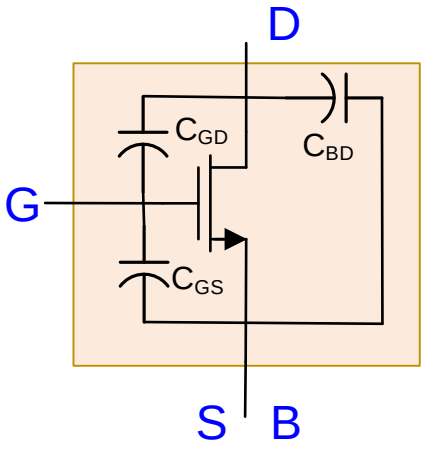


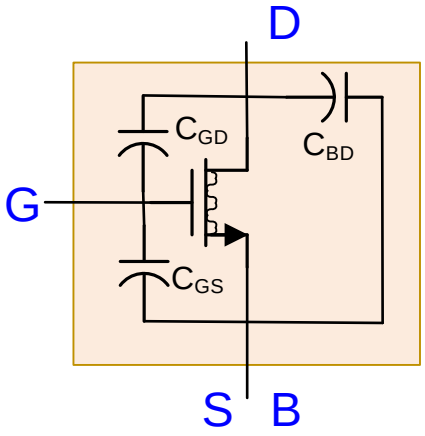
High Frequency Large Signal Model



High Frequency Small Signal Model

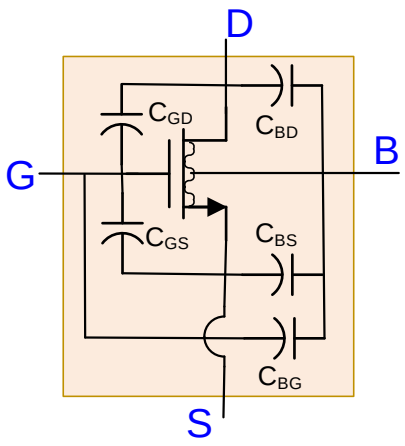
Often V_{BS}=0 and C_{BG}=0, so simplifies to

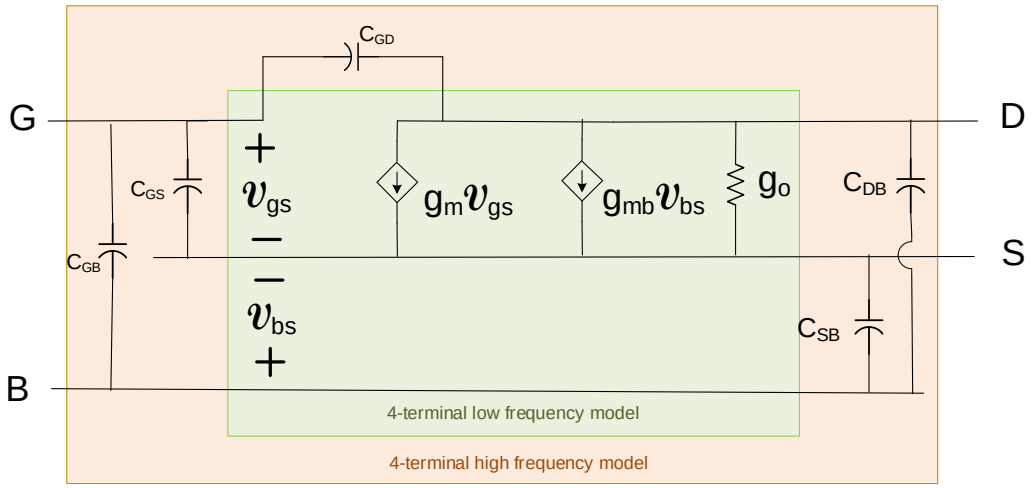




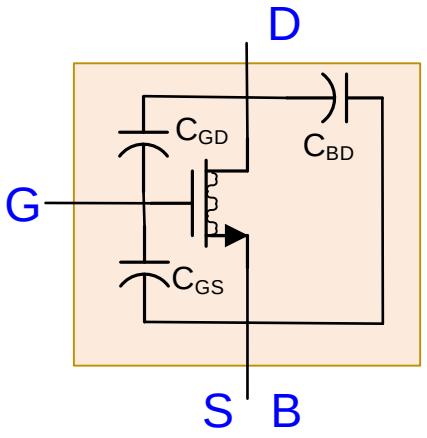
Review from Last Lecture

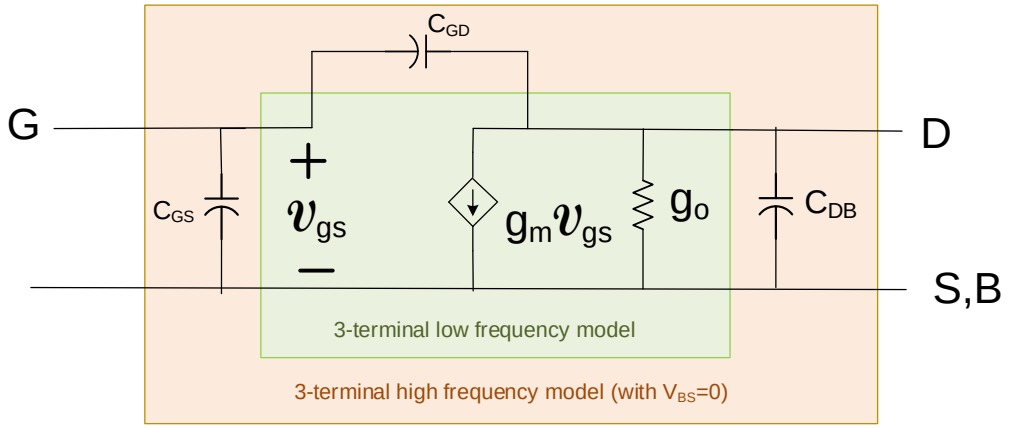
High Frequency Small-Signal Model





Often V_{BS}=0 and C_{BG}=0, so simplifies to

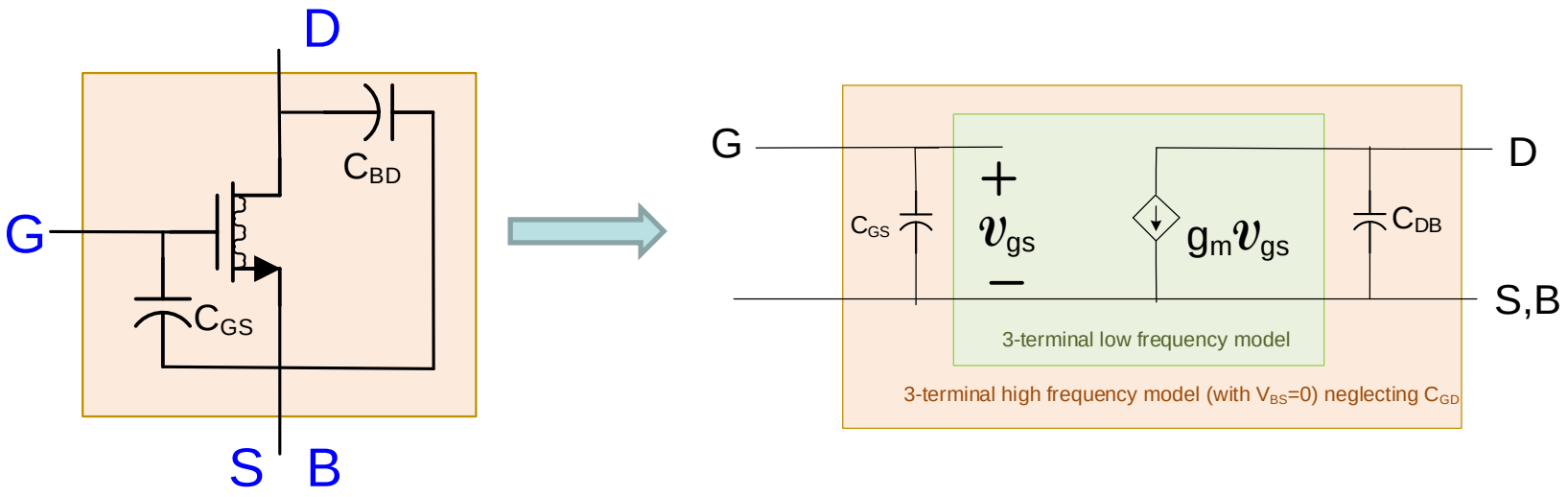




Review from Last Lecture

High Frequency Small-Signal Model

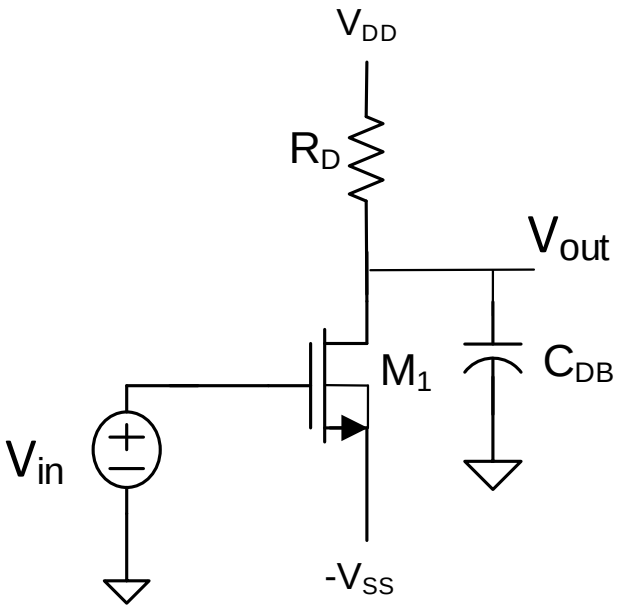
Often V_{BS}=0 and C_{BG}=0 and C_{GD} and g_0 can be neglected so simplifies farther to

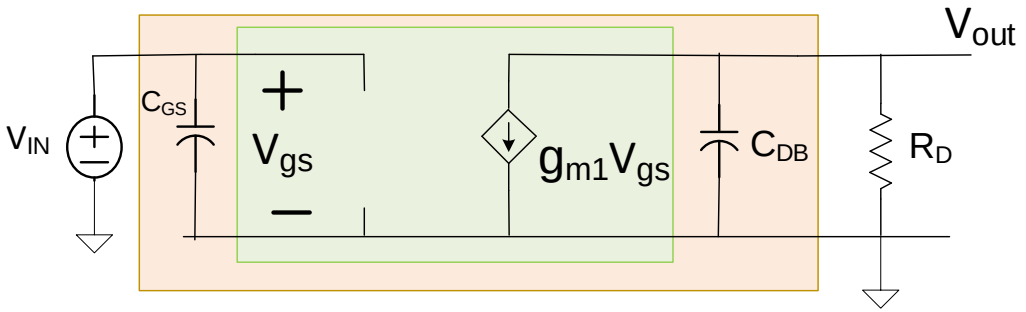


Neglecting C_{GD} which is high frequency feedback from output to input often simplifies analysis considerably

Amplifiers with Small Capacitors

Consider parasitic C_{GS} and C_{DB}





By KCL: (since impedance of C_{DB}= $\frac{1}{sC_{DB}}$)

$$v_{OUT}\left(sC_{DB}+G_D\right)=-g_{m1}v_{IN}$$

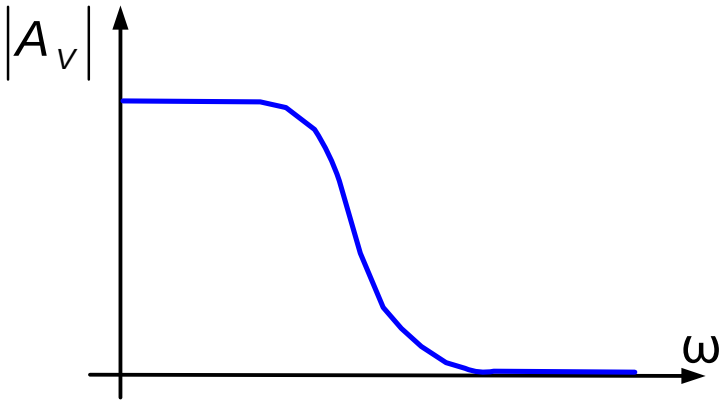
Causes gain to decrease at high frequencies

Solving:

$$\frac{v_{OUT}}{v_{IN}}=\frac{-g_{m1}}{sC_{DB}+G_D}$$

Equivalently:

$$\frac{v_{OUT}}{v_{IN}}=\frac{-g_{m1}R_D}{sC_{DB}R_D+1}$$



Response to Student Question from Last Lecture:

f_T and f_{MAX} for a semiconductor process

f_T is defined to be the frequency where the short-circuit current gain of a transistor drops to unity

f_{MAX} is defined to be the frequency where the power gain of the transistor drops to unity (related to the maximum frequency of oscillation in a process)

$$f_T \simeq \frac{3}{4\pi}\frac{\mu V_{EB}}{L_{min}^2} = \frac{3}{16\pi}\frac{\mu\left|V_{DD}-V_{TH}\right|}{(\lambda - LD)^2}$$

f_T strongly dependent on V_{EB}

for the ON 0.5u process

u_nC_{OX}=100uA/V^2
C_{OX}=2.4fF/u^2
λ=0.2u
LD=.05u
V_{THn}=0.8V

u_n=4E10$_{A\mu^2F^{-1}V^{-2}}$
u_n=400$_{cm^2AF^{-1}V^{-2}}$

At V_{EB}=1V, f_T=25GHz

Note: As feature sizes shrink with process nodes, $V_{EB\text{-}MAX}$ will typically drop linearly but L_{min} will drop quadratically thus f_T gets much larger in small feature processes

Response to Student Question from Last Lecture:

f_T and f_{MAX} for a semiconductor process

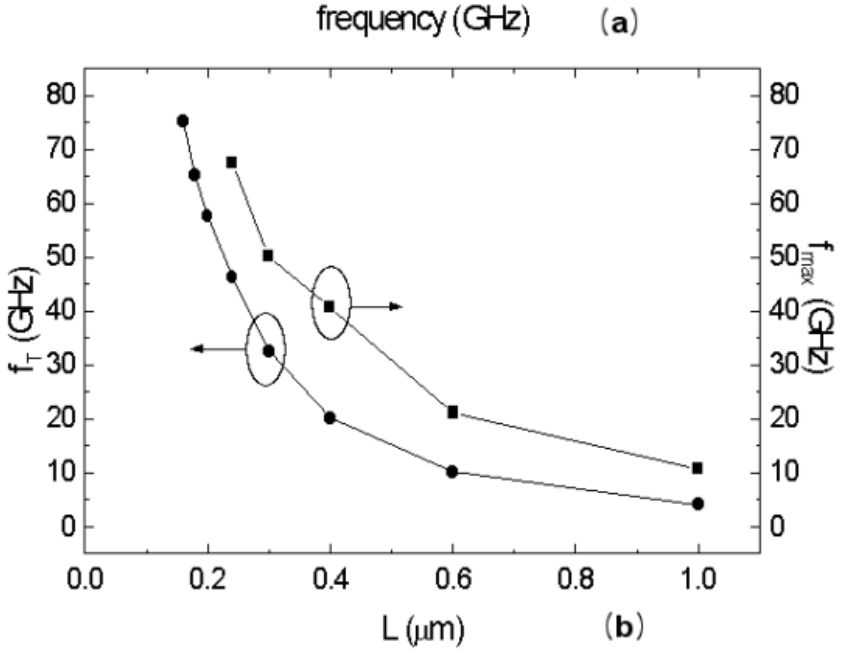


Fig. 7. (a) Maximum stable gain (MSG) and maximum available gain (MAG) for different channel lengths and (b) the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) as functions of the channel length.

For 0.18u process, V_D=2V, V_G=1.2V

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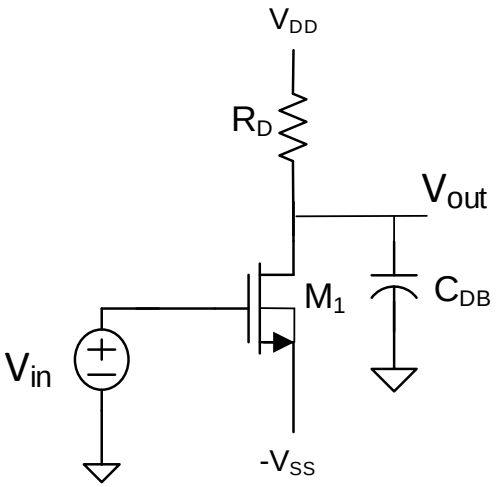
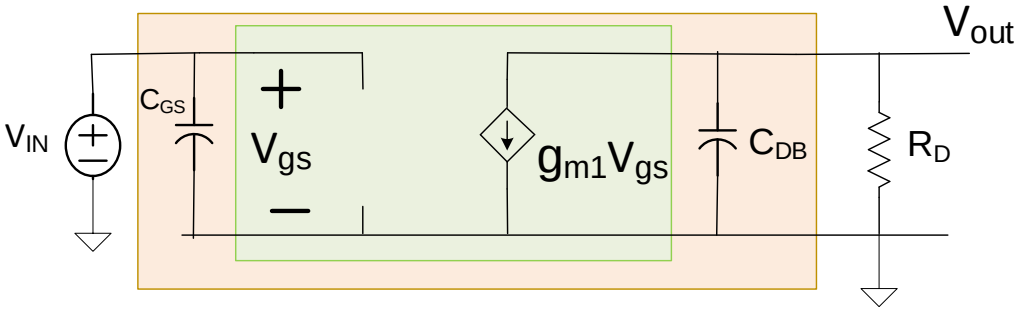
Amplifiers with Small Capacitors

Consider parasitic C_{GS} and C_{DB}



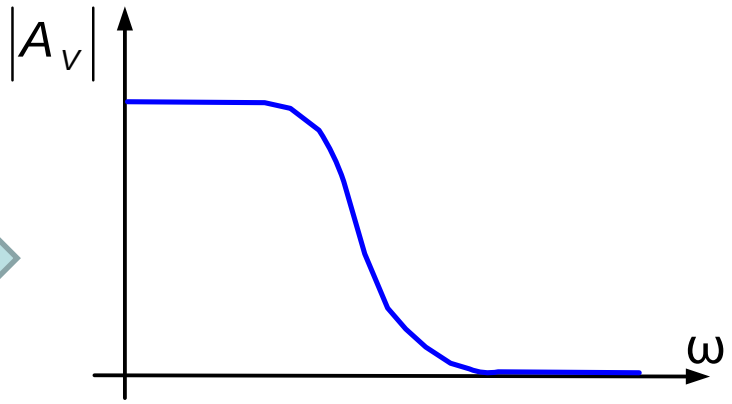


$$\frac{v_{OUT}}{v_{IN}} = A_V(s) = -\frac{-g_{m1}R_D}{sC_{DB}R_D + 1}$$

$$A_V(j\omega) = \frac{-g_{m1}R_D}{j\omega C_{DB}R_D + 1}$$

$$\left|A_V(j\omega)\right| = \frac{g_{m1}R_D}{\sqrt{(\omega C_{DB}R_D) + 1}}$$

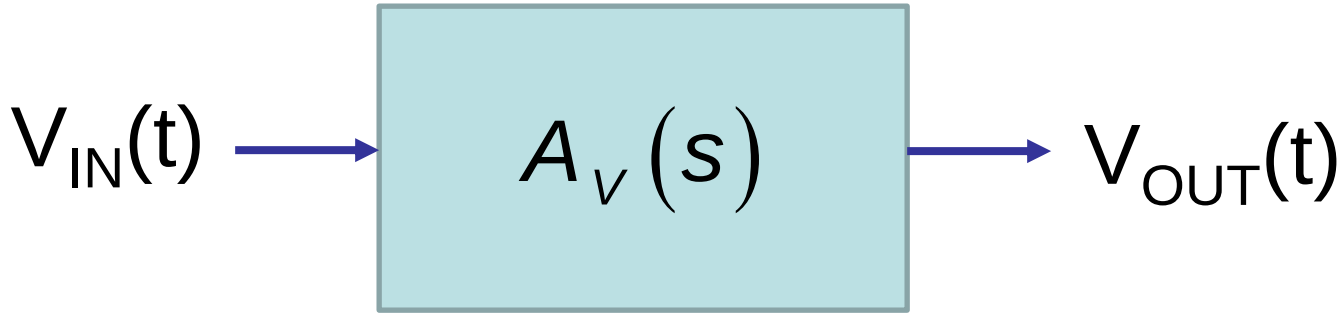
$$\angle A_V(j\omega) = -180^o - \tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)$$



Since first-order low-pass, half-power frequency given by

$$\omega_{3dB} = \frac{1}{R_D C_{DB}}$$

Sinusoidal Steady State Response for Linear Systems



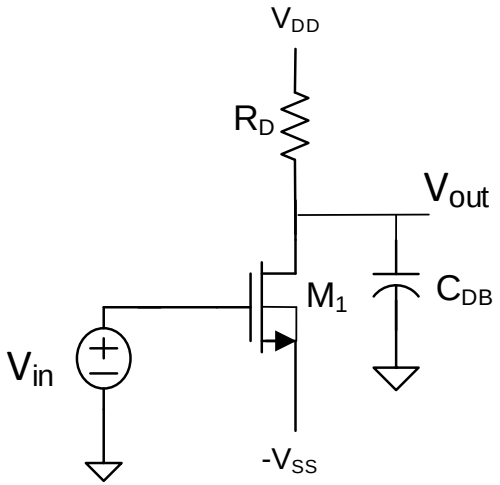
Key Result from EE 201

If $V_{IN}=V_m\sin(\omega t+\theta)$ where V_m is small (so linear operation maintained)

Steady state output is also a sinusoid given by

$$V_{OUT}(t) = V_m \left| A_V(j\omega) \right| \sin\left(\omega t + \theta + \angle A_V(j\omega)\right)$$

Sinusoidal Steady State Response for Linear Systems



$$\left|A_V(j\omega)\right| = \frac{g_{m1}R_D}{\sqrt{\left(\omega C_{DB}R_D\right)^2 + 1}}$$

$$\angle A_V(j\omega) = -180^o - \tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)$$

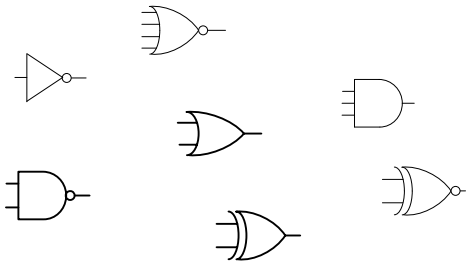
If $V_{IN}=V_m\sin(\omega t+\theta)$

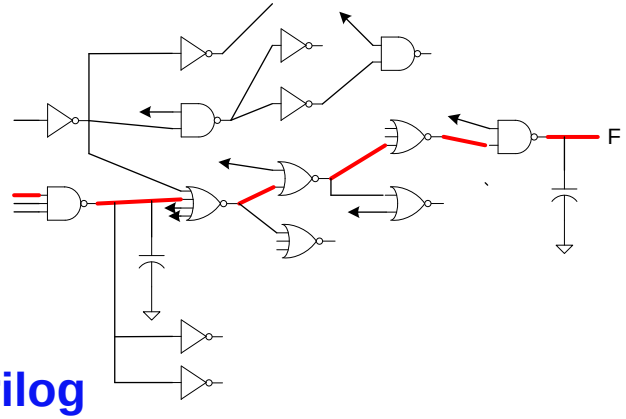
For V_m small, small-signal steady state output given by

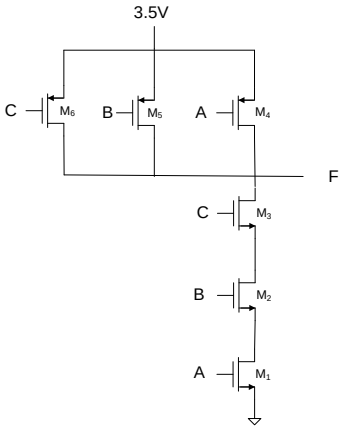
$$V_{OUT}(t) = V_m \frac{g_{m1}R_D}{\sqrt{\left(\omega C_{DB}R_D\right)^2 + 1}} \sin\left(\omega t + \theta - 180^o - \tan^{-1}\left(\frac{\omega C_{DB}R_D}{1}\right)\right)$$

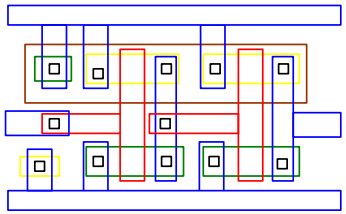
Digital Circuit Design

Most of the remainder of the course will be devoted to digital circuit design







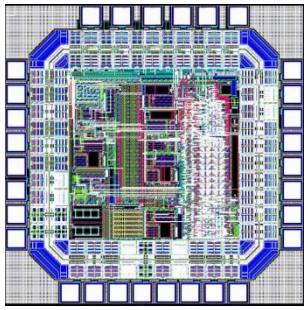


Verilog

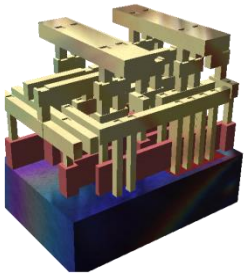
```
module gates (input logic [3:0] a,b,
              output logic [3:0] y1,y2,y3,y4,y5);
  assign y1 = a&b;  //AND
  assign y2 = a | b;  //OR
  assign y3 = a ^ b;  //XOR
  assign y4 = ~(a & b);  //NAND
  assign y5 = ~( a | b);  //NOR
endmodule
```

VHDL

```
library IEEE; use IEEE.STD_LOGIC_1164.all;

entity gates is
   port(a,b: in STD_LOGIC_VECTOR(3 dowto 0);
        y1,y2,y3,y4,y5:out STD_LOGIC_VECTOR(3 downto 0));
end;

architecture synth of gates is
begin

y1 <= a and b;
y2 <= a or b;
y3 <= a xor b;
y4 <= a nand b;
y5 <= a nor b;
end;
```



A rendering of a small standard cell with three metal layers (dielectric has been removed). The sand-colored structures are metal interconnect, with the vertical pillars being contacts, typically plugs of tungsten. The reddish structures are polysilicon gates, and the solid at the bottom is the crystalline silicon bulk

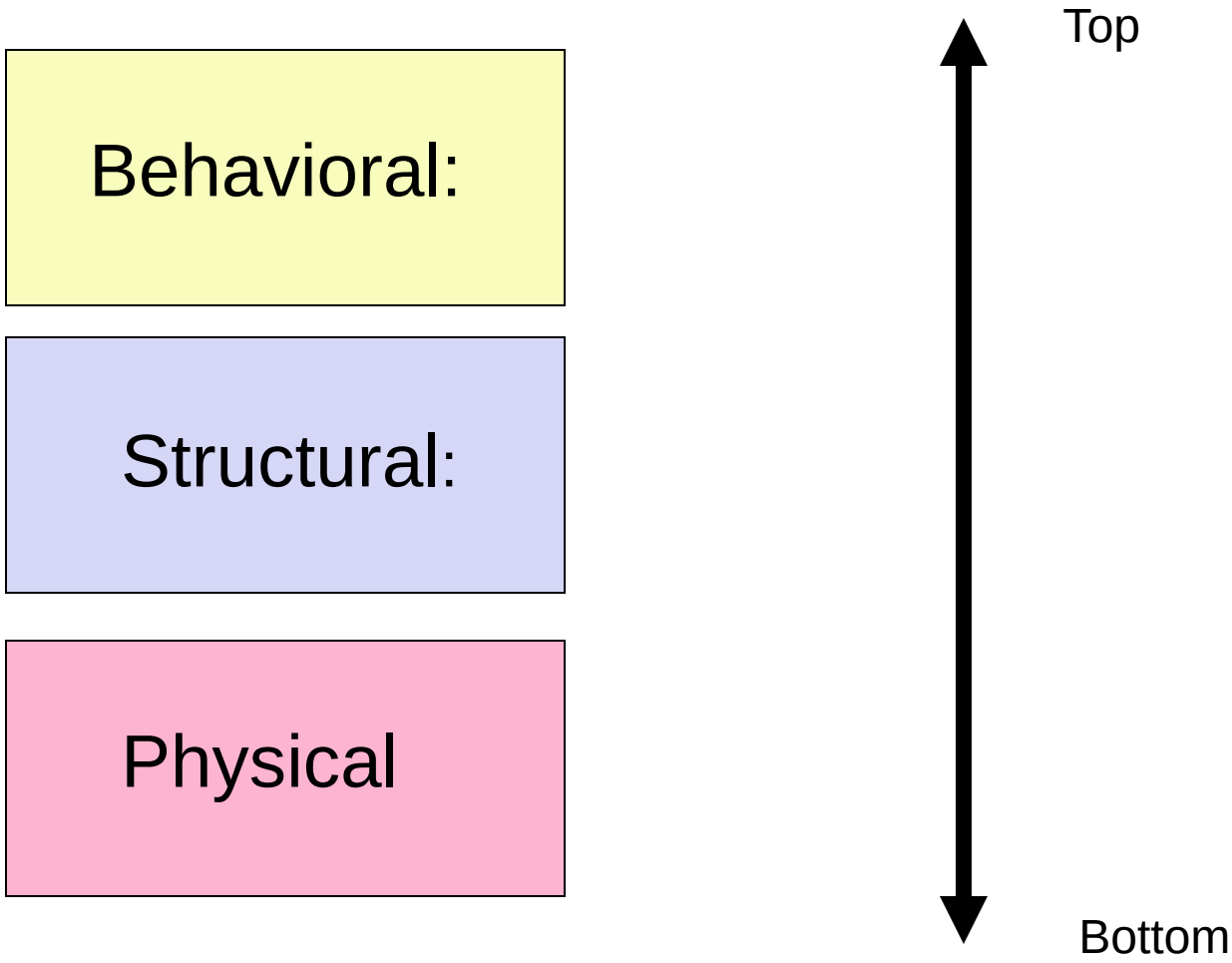


Standard Cell Library

Digital Circuit Design

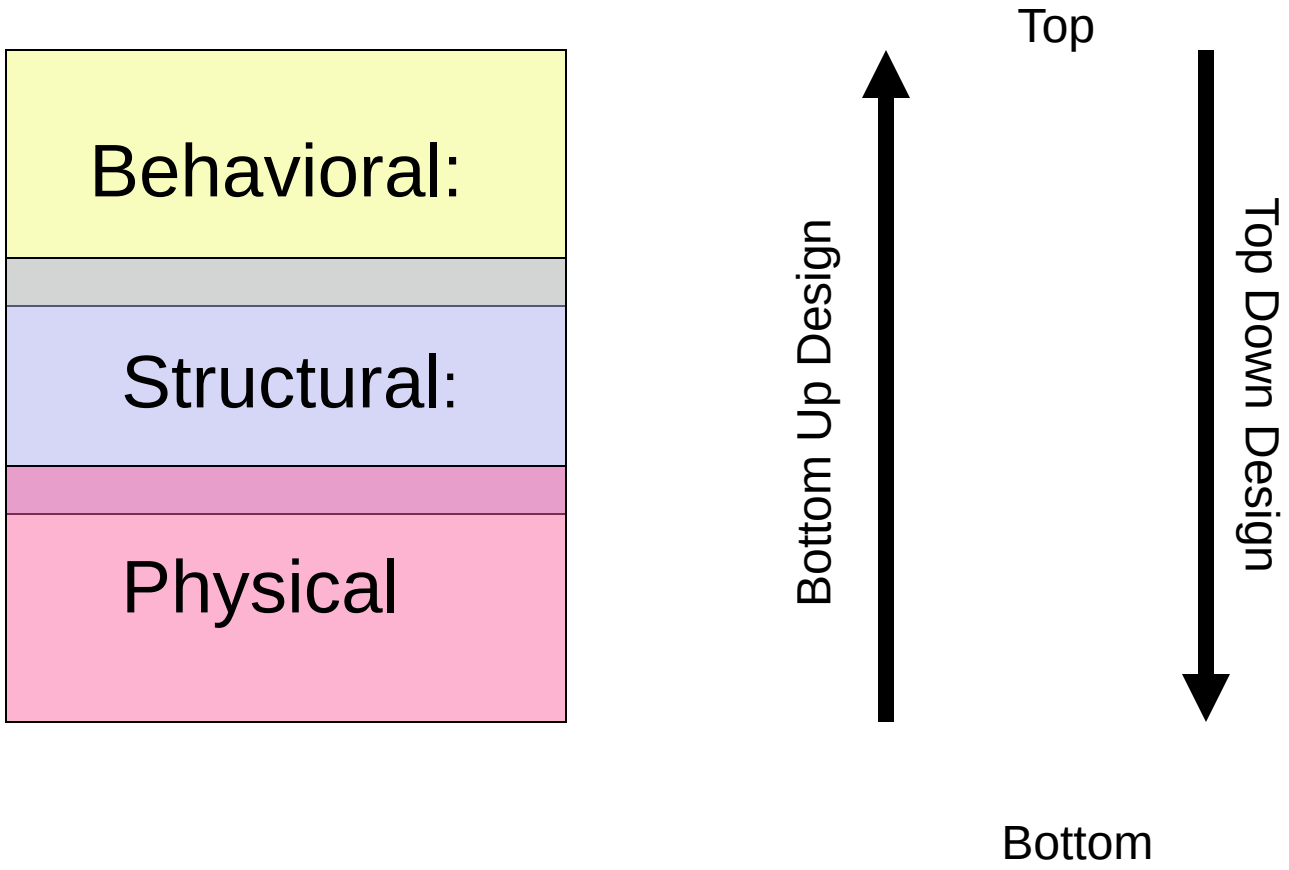
- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
    - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

Hierarchical Digital Design Domains:

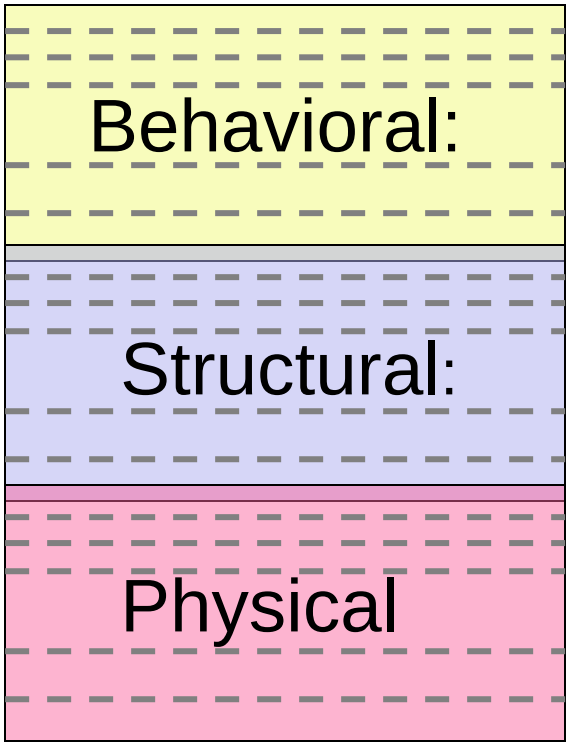


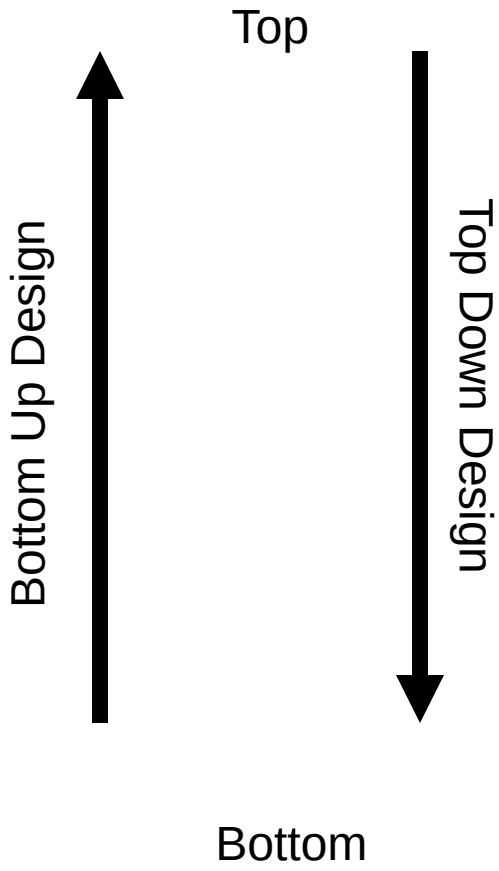
Multiple Levels of Abstraction

Hierarchical Digital Design Domains:



Hierarchical Digital Design Domains:





Multiple Sublevels in Each Major Level

All Design Steps may not Fit Naturally in this Description

Hierarchical Digital Design Domains:

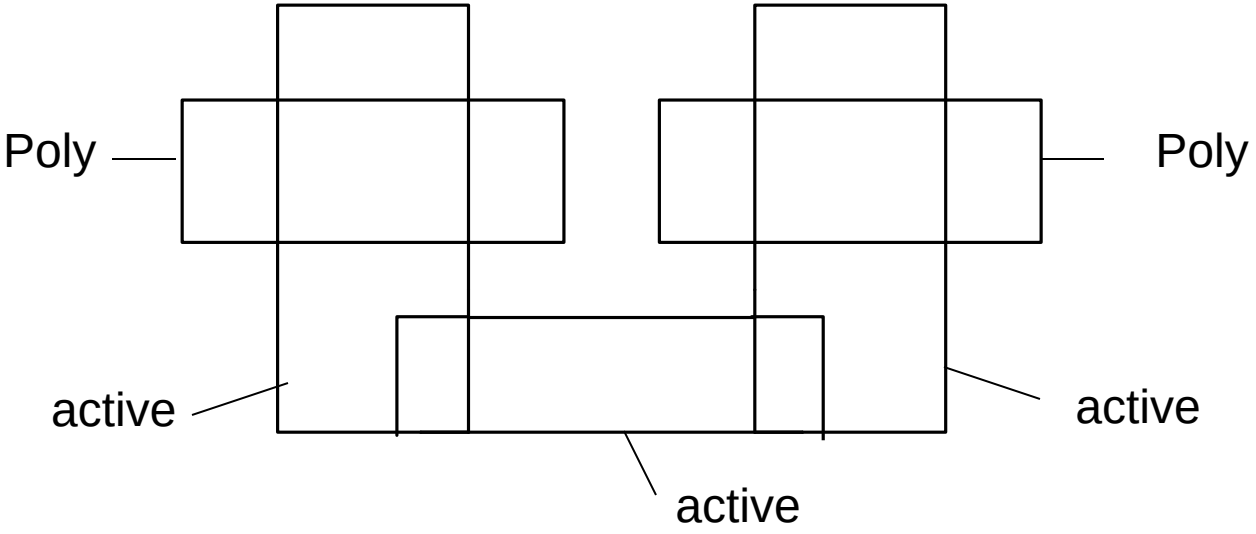
Behavioral : Describes what a system does or what it should do

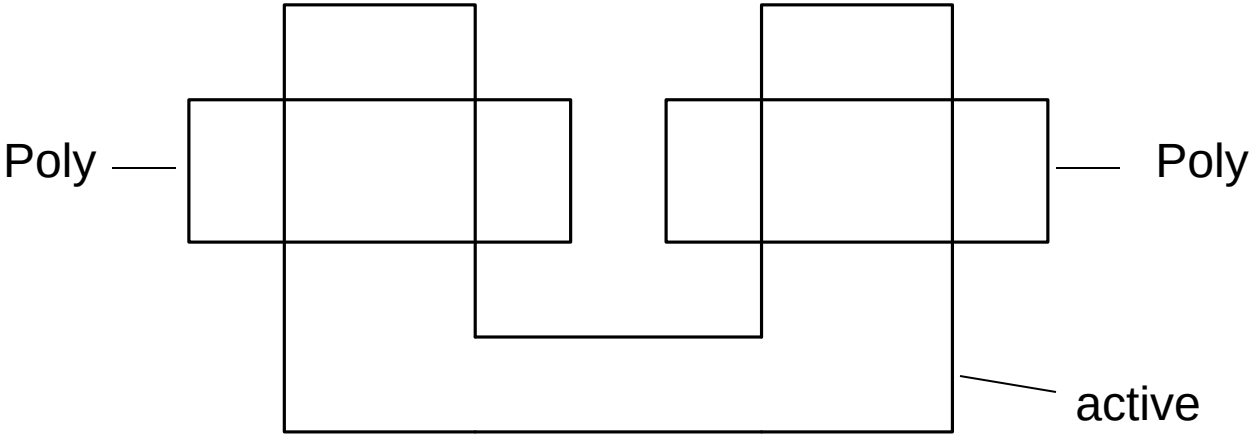
Structural : Identifies constituent blocks and describes how these blocks are interconnected and how they interact

Physical : Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

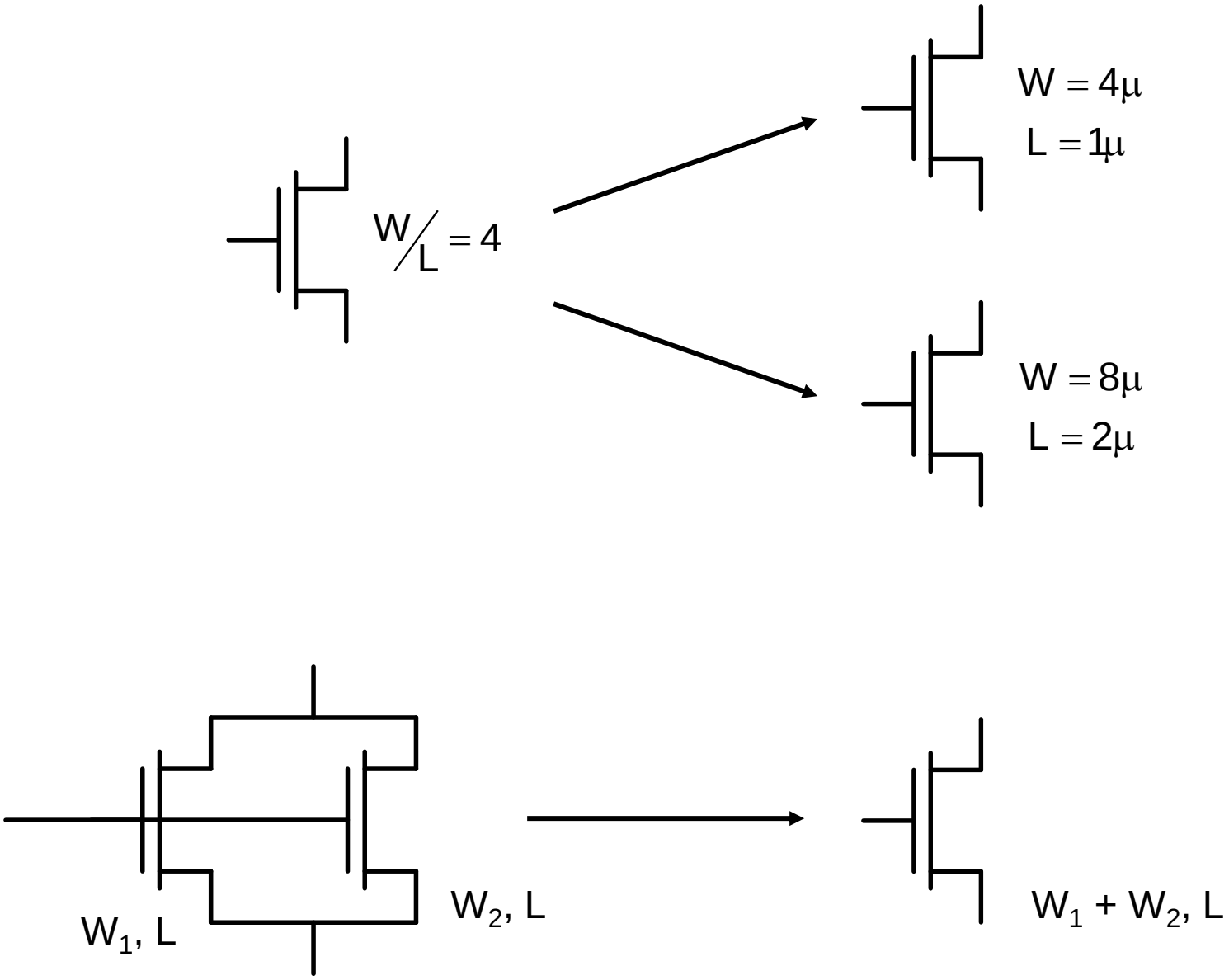
Multiple representations often exist at any level or sublevel

Example: Two distinct representations at the physical level (polygon sublevel)

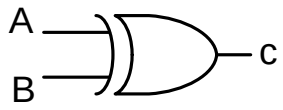




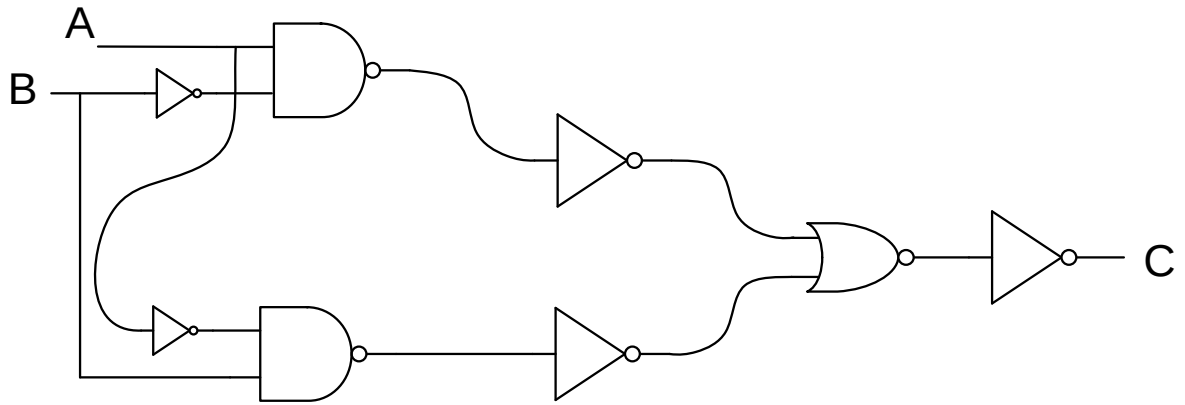
Example: Two distinct representations at physical level (schematic sublevel)

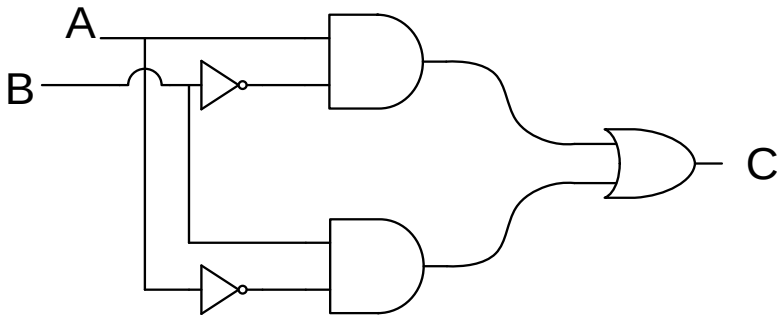


Example: Three distinct representations at the structural/behavioral level (gate sublevel)



$$C = A \oplus B$$





In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

– Consider lowest level to highest

0 - placement of diffusions, thin oxide regions, field oxide, ect. on a substrate.

1 - polygons identify all mask information (not unique)

2 - transistors (not unique)

3 - gate level (not unique)

4 - cell level Adders, Flip Flop, MUTs,…

Information Type

PG data
G.D.F
Netlist
HDL Description

Structural Domain:

- DSP
- Blocks (Adders, Memory, Registers, etc.
- Gates
- Transistor

Information Type

HDL

Netlists

Behavior Domain (top down):

- Application
- Programs
- Subroutines
- Boolean Expressions

Information Type

High-Level Language
HDL

Representation of Digital Systems

Standard Approach to Digital Circuit Design

8 – level representation

1. Behavioral Description
   - Technology independent
2. RTL Description (Register Transfer Level)

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis

   Generally use a standard call library for synthesis

(sublevels 6-8 not shown on this slide)

Frontend design

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description
   - Technology independent
2. RTL Description

   (must verify (1) ⇔ (2))
3. RTL Compiler

   Registers and Combinational Logic Functions
4. Logic Optimizer

5. Logic Synthesis

   Generally use a standard call library for synthesis

Backend design

6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   - DRC
   - Back Annotation
8. Post Layout simulation

   May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles

Logic Optimization

What is optimized (or minimized) ?

- Number of Gates
- Number or Levels of Logic
- Speed
- Delay
- Power Dissipation
- Area
- Cost
- Peak Current
- • •

Depends Upon What User Is Interested In

Standard Cell Library

- Set of primitive building blocks that have been pre-characterized for dc and high frequency performance
- Generally includes basic multiple-input gates and flip flops
- P-cells often included
- Can include higher-level blocks
  - Adders, multipliers, shift registers,counters,…
- Cell library often augmented by specific needs of a group or customer

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- Propagation Delay with Multiple Levels of Logic
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- Ring Oscillators

---

done

partial

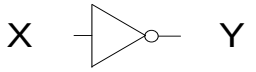
Logic Circuit Block Design

Many different logic design styles

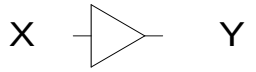
- Static Logic Gates
- Complex Logic Gates
- Pseudo NMOS
- Pass Transistor Logic
- Dynamic Logic Gates
  - Domino Logic
  - Zipper Logic
  - Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block

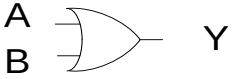
The basic logic gates



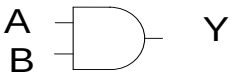
$$Y = \overline{X}$$



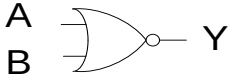
$$Y = X$$



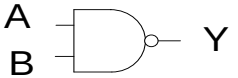
$$Y = A + B$$



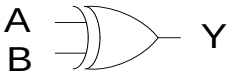
$$Y = A \bullet B$$



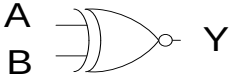
$$Y = \overline{A + B}$$



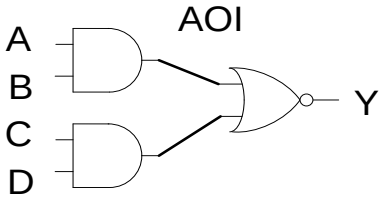
$$Y = \overline{A \bullet B}$$



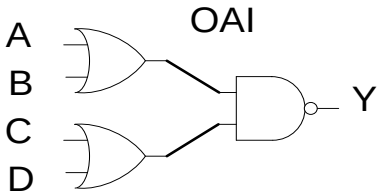
$$Y = A \oplus B$$



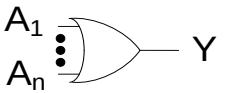
$$Y = \overline{A \oplus B}$$



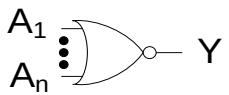
$$Y = \overline{A \bullet B + C \bullet D}$$



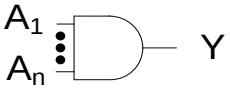
$$Y = \overline{(A + B) \bullet (C + D)}$$



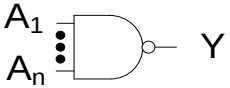
$$Y = A_1 + A_2 + \ldots A_n$$



$$Y = \overline{A_1 + A_2 + \ldots A_n}$$

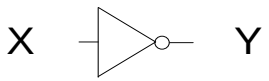


$$Y = A_1 \bullet A_2 \bullet \ldots A_n$$

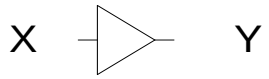


$$Y = \overline{A_1 \bullet A_2 \bullet \ldots A_n}$$

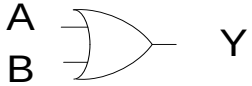
The basic logic gates



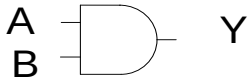
$$Y = \overline{X}$$



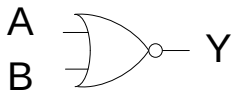
$$Y = X$$



$$Y = A + B$$



$$Y = A \bullet B$$



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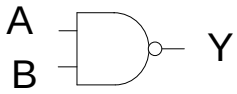
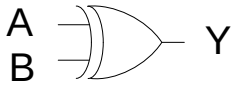


$$Y = \overline{A \bullet B}$$



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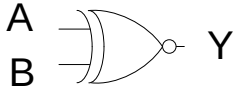


$$Y = \overline{A \oplus B}$$

Question: How many basic one and two input gates exist and how many of these are useful?

The basic logic gates

The set of NOR gates is complete

Any combinational logic function can be realized with only multiple-input NOR gates

The set of NAND gates is complete

Any combinational logic function can be realized with only multiple-input NAND gates

Performance of the BASIC gates is critical!

The basic logic gates

A gate logic family can be formed based upon a specific design style for implementing logic functions

Many different gate logic family types exist

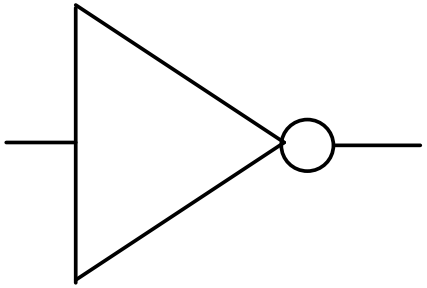
NMOS, PMOS, CMOS, TTL, ECL, RTL, DCTL,…

Substantial differences in performance from one family type to another

Power, Area, Noise Margins, ….

The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.



What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

What restrictions are there on the designer for building Boolean circuits?

- None !!!!
- It must “work” as expected
- Designer is Master of the silicon !

Desirable and/or Required Logic Family Characteristics

What are the desired characteristics of a logic family?

Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
9. Low leakage currents
10. No oscillations during transitions
11. Compatible with synthesis tools
12. Characteristics do not degrade too much with temperature
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate
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Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

Desirable and/or Required Logic Family Characteristics

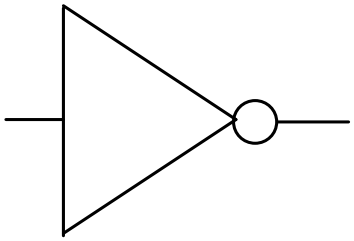
Are some of these more important than others?

Yes ! – must have well-defined logic levels for circuits to even function as logic

What properties of an inverter are necessary for it to be useful for building a logic family

What are the logic levels for a given inverter of for a given logic family?

What are the logic levels for a given inverter of for a given logic family?



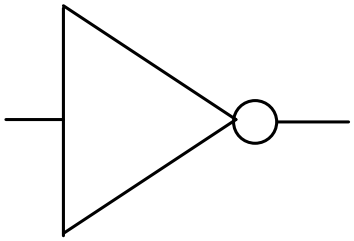
V_H=?

V_L=?

Can we legislate them ?

- Some authors choose to simply define a value for them
- Simple and straightforward approach
- **But what if the circuit does not interpret them the same way they are defined !!**

What are the logic levels for a given inverter of for a given logic family?



V_H=? V_L=?

Can we legislate them ?

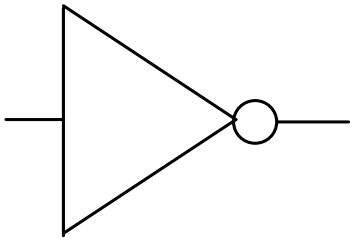
In 1897 the Indiana House of Representatives unanimously passed a measure redefining the area of a circle and the value of pi. (House Bill no. 246, introduced by Rep. Taylor I. Record.) The bill died in the state Senate.

Indiana Pi Bill

From Wikipedia, the free encyclopedia

The **Indiana Pi Bill** is the popular name for bill #246 of the 1897 sitting of the Indiana General Assembly, one of the most notorious attempts to establish mathematical truth by legislative fiat. Despite its name, the main result claimed by the bill is a method to square the circle, although it does imply various incorrect values of the mathematical constant π, the ratio of the circumference of a circle to its diameter.[1] The bill, written by a physician who was an amateur mathematician, never became law due to the

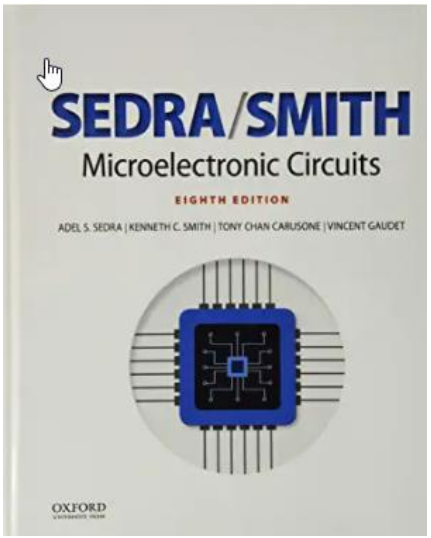
What are the logic levels for a given inverter of for a given logic family?



V_H=?

V_L=?

Can we legislate them ?



World's most widely used electronics text

Noise Margins The static operation of a logic-circuit family is characterized by the voltage transfer characteristic (VTC) of its basic inverter. Figure 10.2 shows such a VTC and defines its four parameters; V_{OH}, V_{OL}, V_{IH}, and V_{IL}. Note that V_{IH} and V_{IL} are defined as the points at which the slope of the VTC is –1. Also indicated is the definition of the threshold voltage V_M, or V_{th} as we shall frequently call it, as the point at which $v_O = v_I$. Recall that we discussed the VTC in its generic form in Section 1.7, and have also seen actual VTCs in Section 4.10 for the CMOS inverter, and in Section 5.10 for the BJT inverter.

The **robustness** of a logic-circuit family is determined by its ability to reject noise, and thus by the noise margins NH_H and NM_L,

$$NM_H \equiv V_{OH} - V_{IH} \quad (10.1)$$

$$NM_L \equiv V_{IL} - V_{OL} \quad (10.2)$$

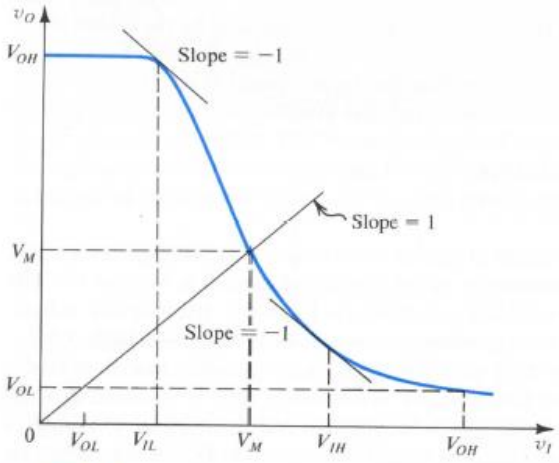
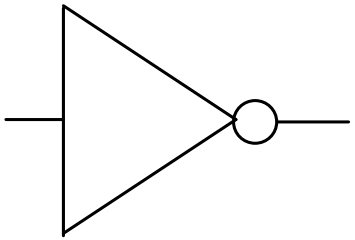


FIGURE 10.2 Typical voltage transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points.

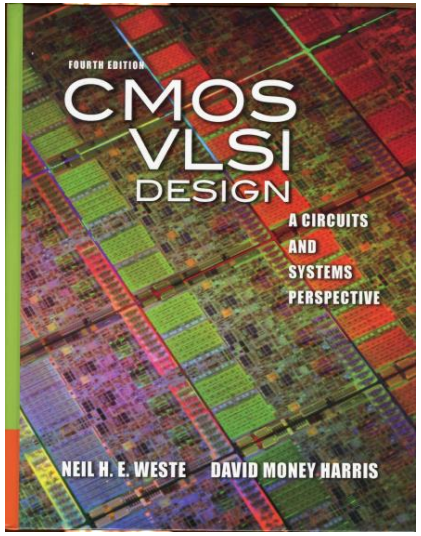
What are the logic levels for a given inverter of for a given logic family?



V_H=?

V_L=?

Can we legislate them ?



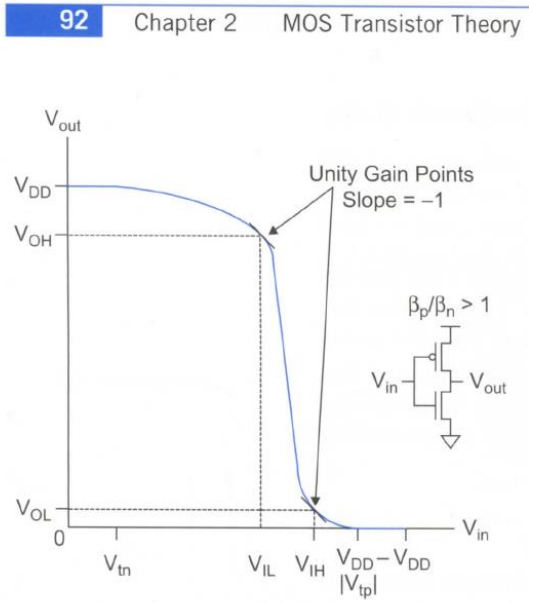
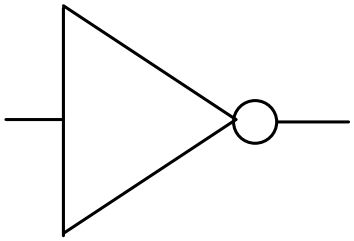


FIGURE 2.30 CMOS inverter noise margins

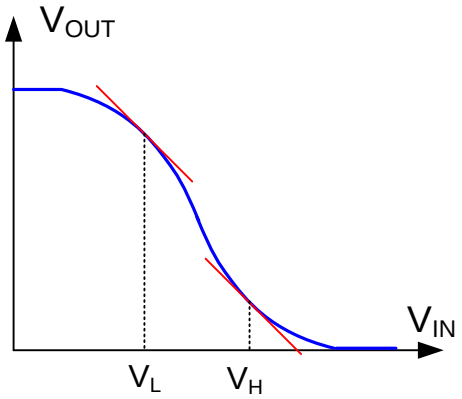
What are the logic levels for a given inverter of for a given logic family?



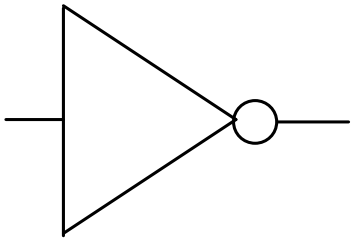
V_H=? V_L=?

Can we legislate them ?

- Some authors choose to define them based upon specific features of inverter
- Analytical expressions may be complicated
- But what if the circuit does not interpret them the same way they are defined !!



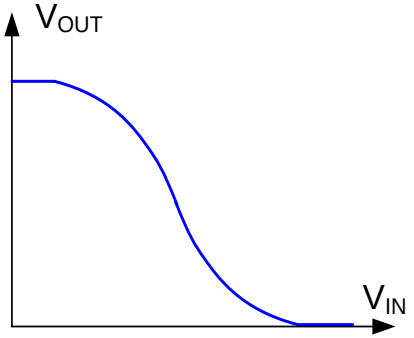
What are the logic levels for a given inverter of for a given logic family?



V_H=? V_L=?

Ask the inverter how it will interpret logic levels

- The inverter <u>will</u> interpret them the way the circuit really operate as a Boolean system !!
- Analytical expressions may be complicated
- How is this determination made?



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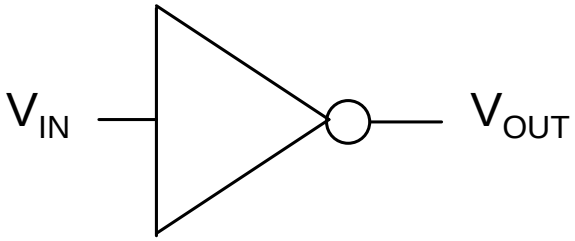
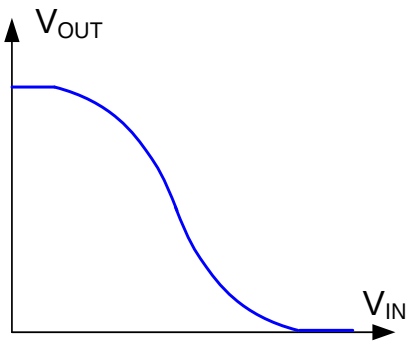


V_H=?

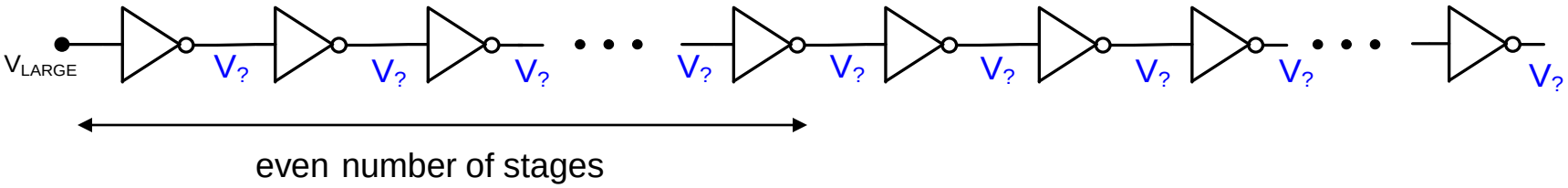
V_L=?



Consider a very long cascade of inverters

Apply a large voltage at the input (alternatively a small input could be used)

w.l.o.g. assume an even number of inverters in chain indicated



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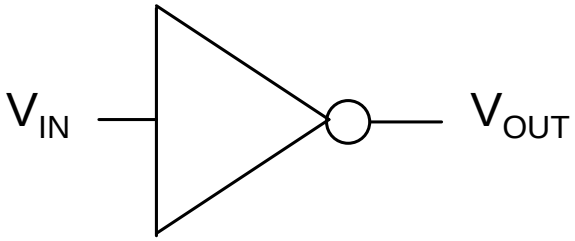
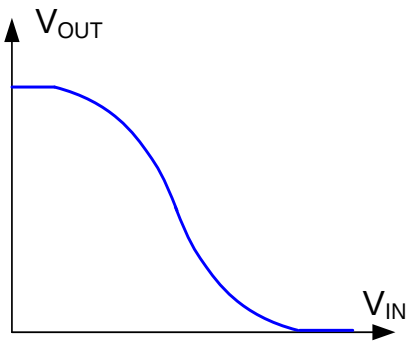


V_H=?

V_L=?



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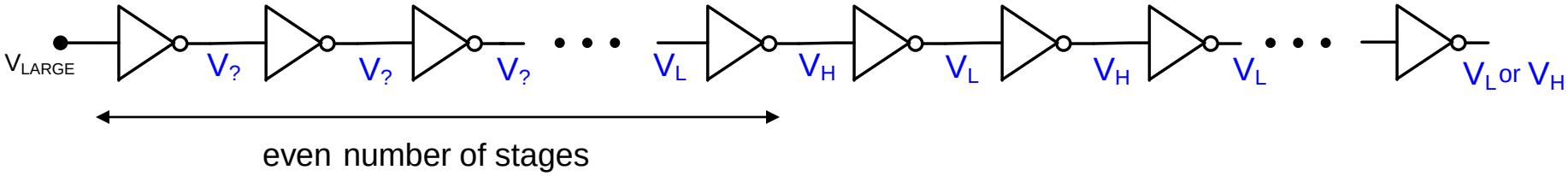
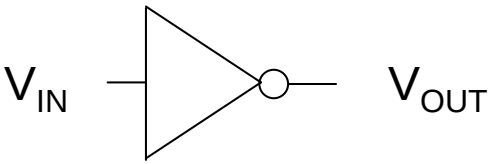


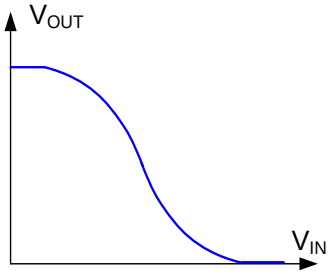
If logic levels are to be maintained, the voltage at the end of this even number of stages must be V_H, that of the next must be V_L, the next V_H, etc. until the start of the cascade is approached

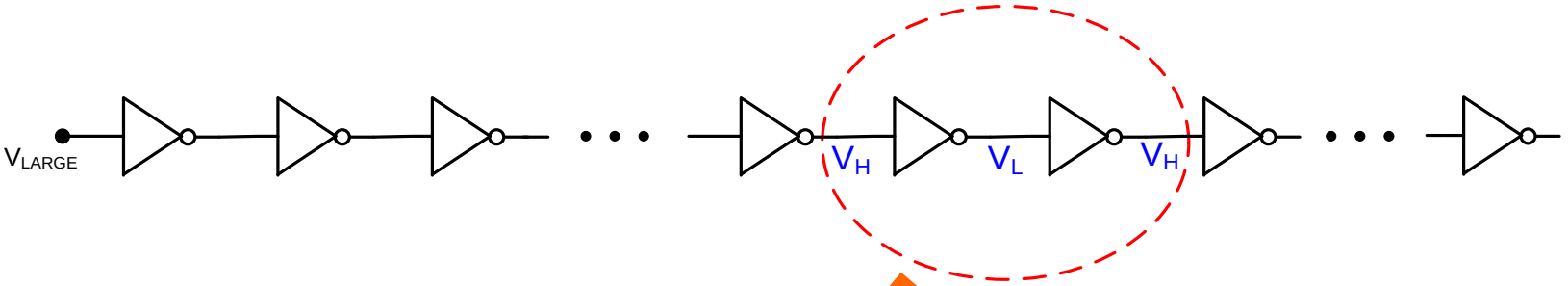
Ask the inverter how it will interpret logic levels

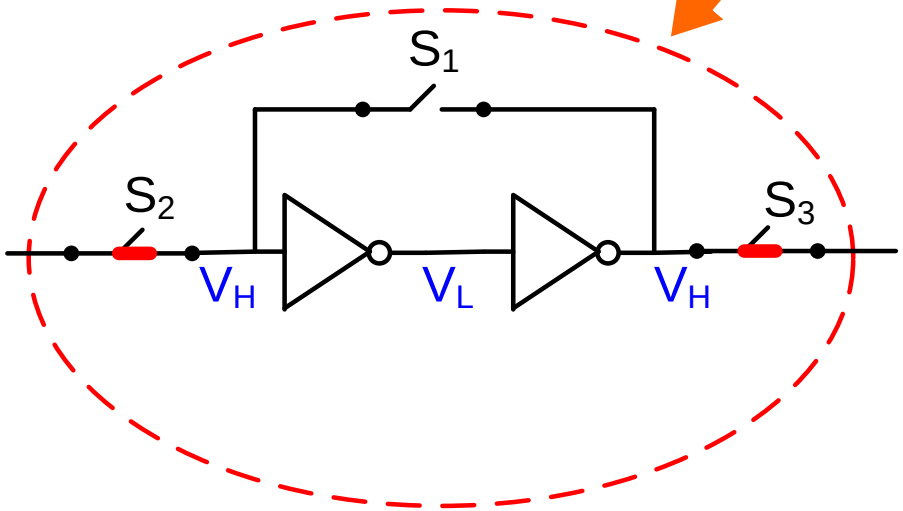


V_H=?

V_L=?







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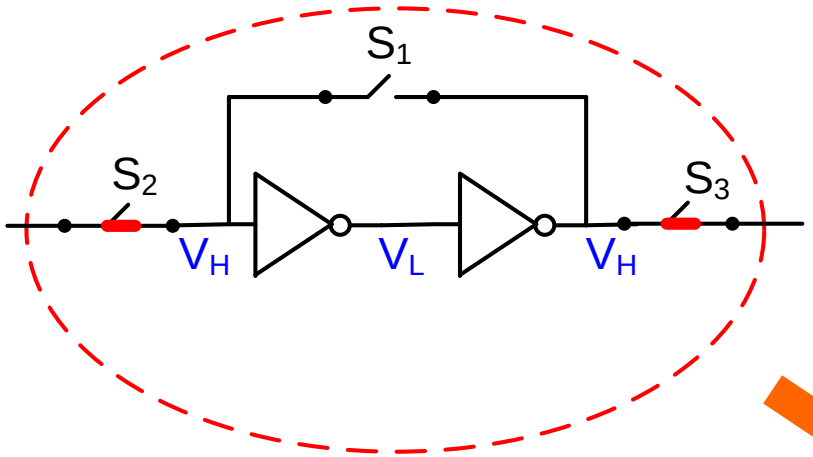
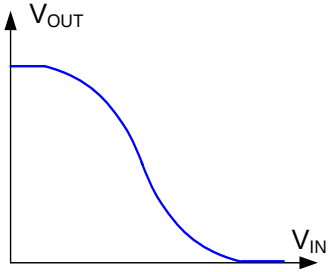
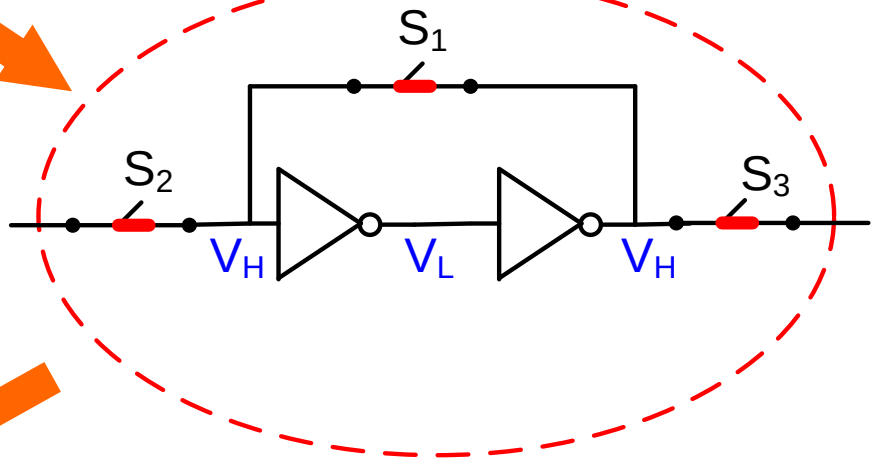
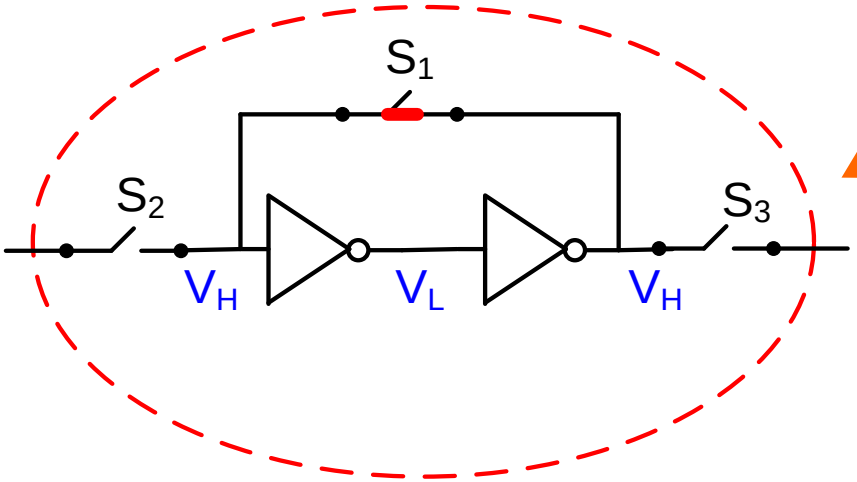




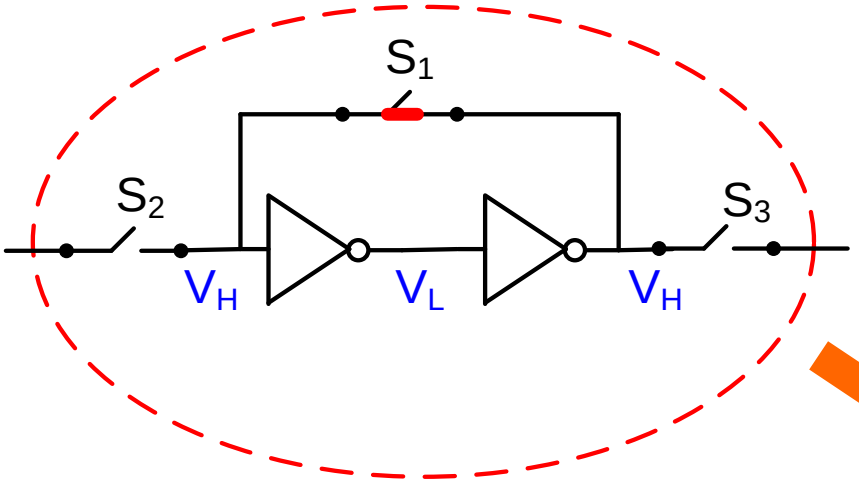
V_H=?

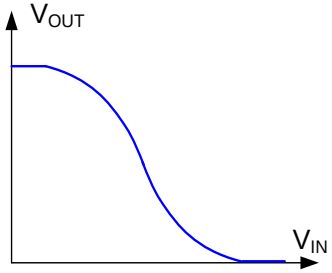
V_L=?





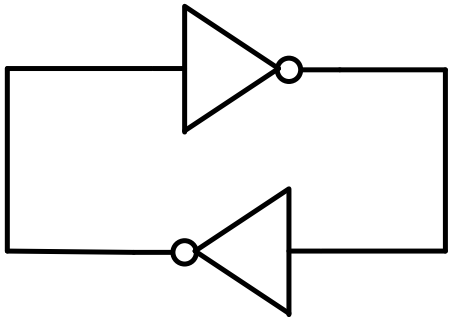
Ask the inverter how it will interpret logic levels





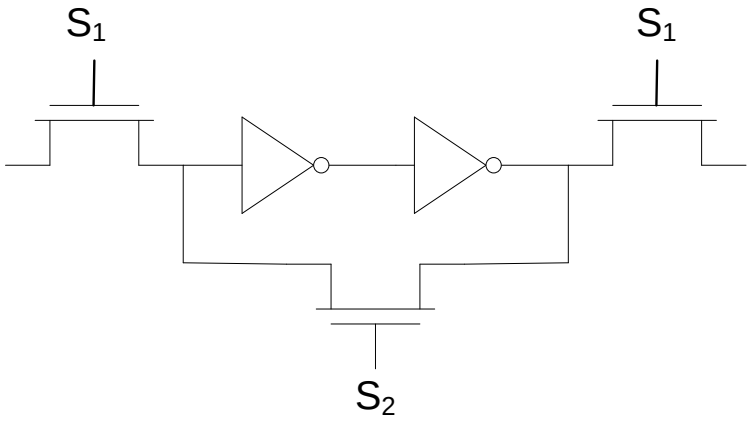
V_H=?

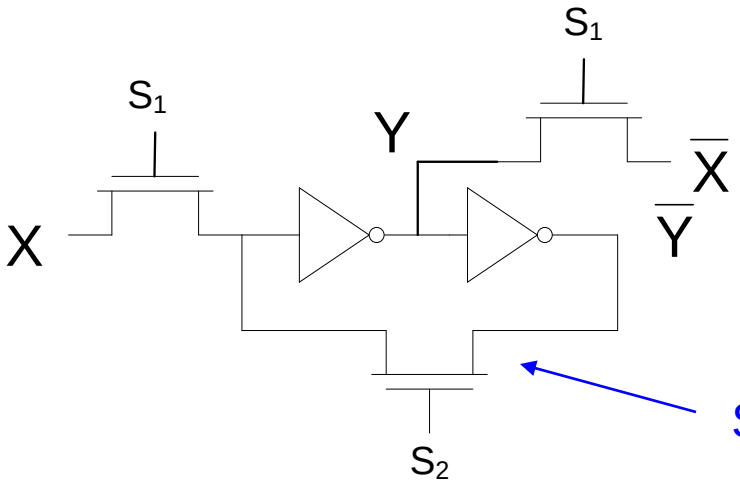
V_L=?



- Two inverter loop
- Very useful circuit !

The two-inverter loop

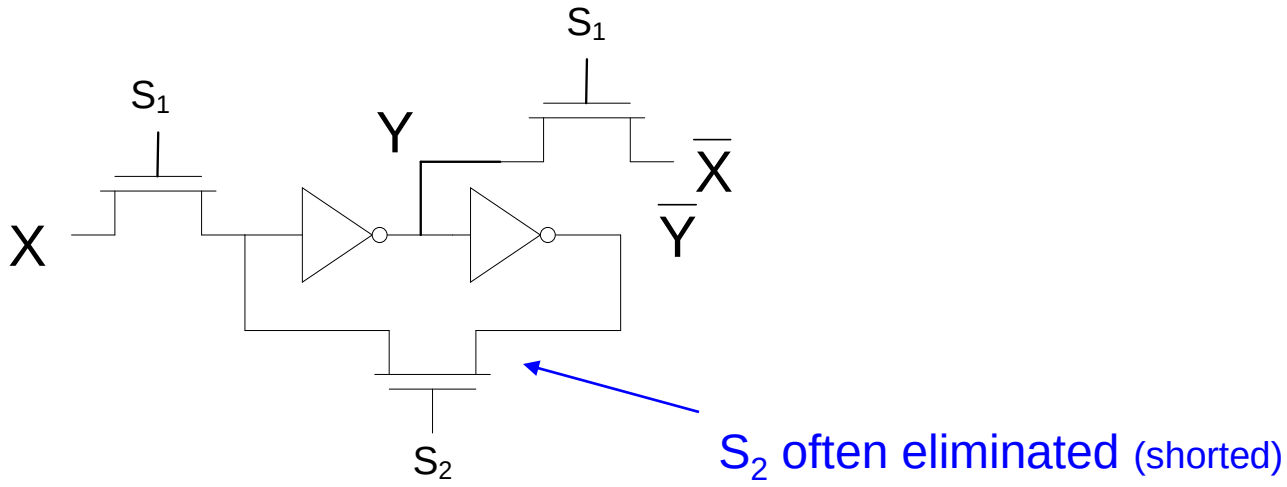


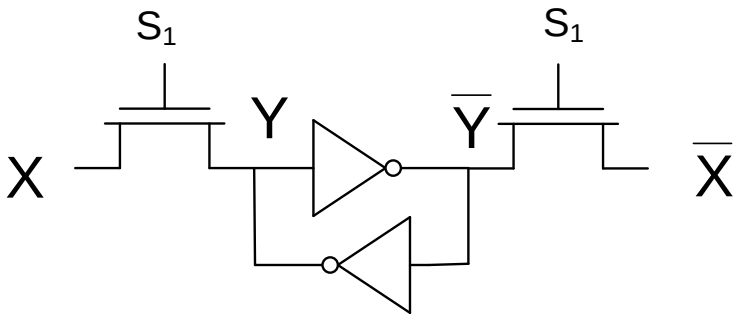


S_2 often eliminated (shorted)

SRAM Cell

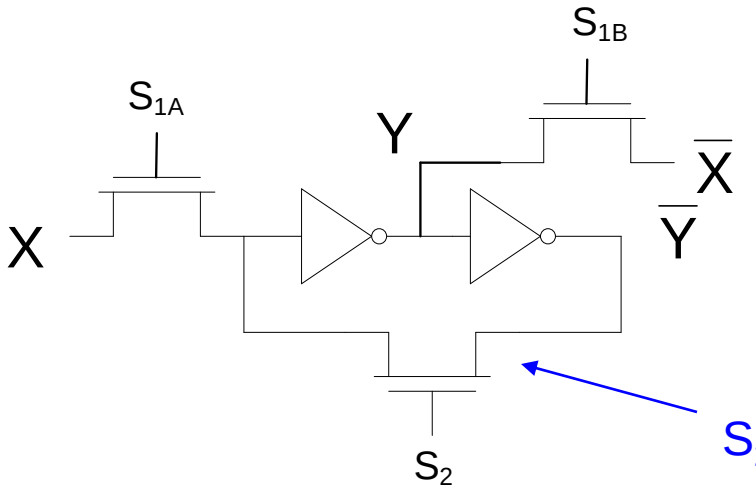
The two-inverter loop





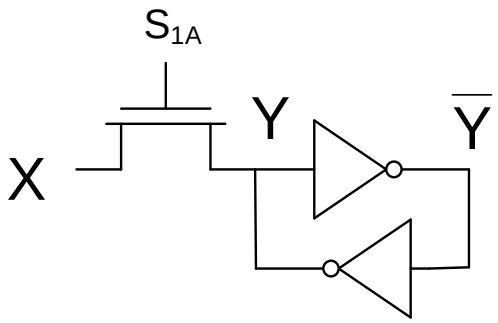
Standard 6-transistor SRAM Cell

The two-inverter loop



S_{1B} can also be eliminated (opened)

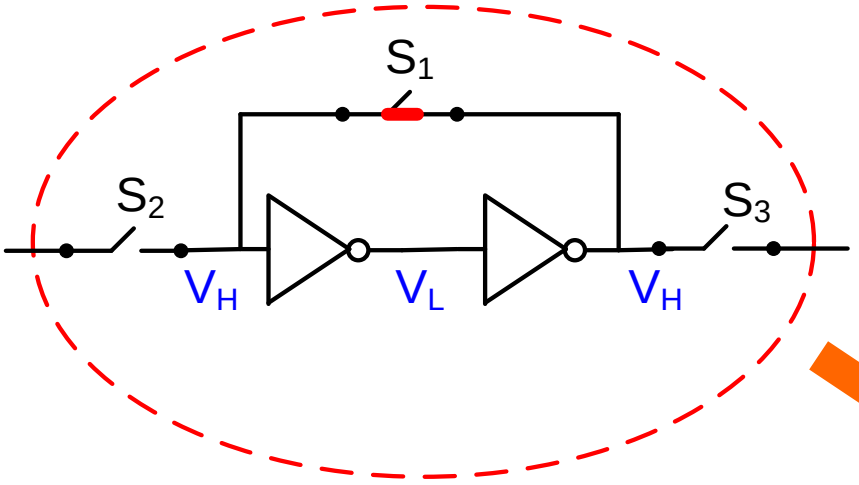
S_2 often eliminated (shorted)

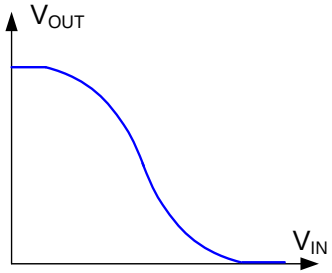


5-transistor SRAM Cell

Will also work but less common (less area but degraded performance)

Ask the inverter how it will interpret logic levels

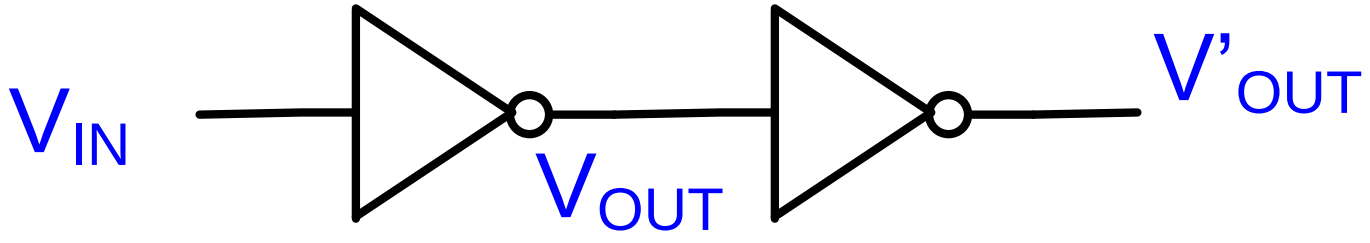




V_H=?

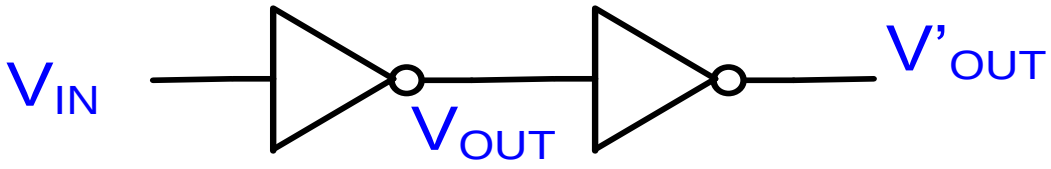
V_L=?

Inverter Characteristics

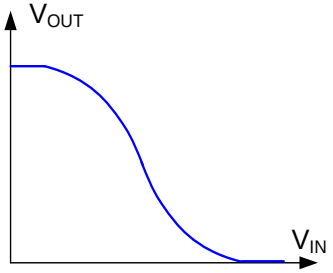


Thus, consider the inverter pair

Ask the inverter how it will interpret logic levels



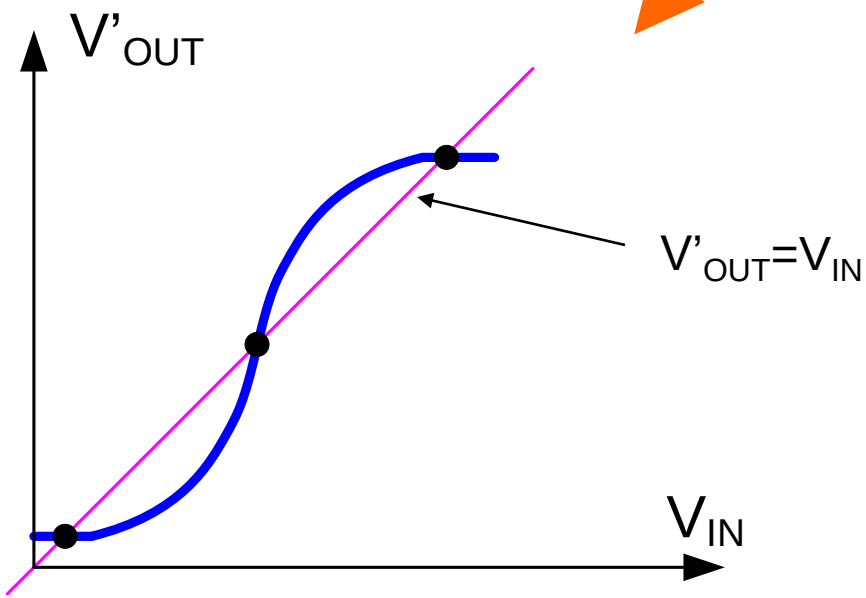
Inverter pair



V_H=?

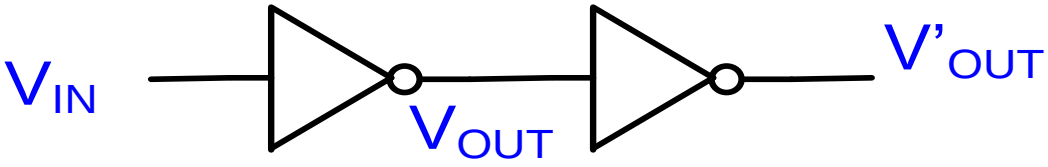
V_L=?

V_H and V_L will be on the intersection of the transfer characteristics of the inverter pair (IPTC) and the $V'_{OUT}=V_{IN}$ line

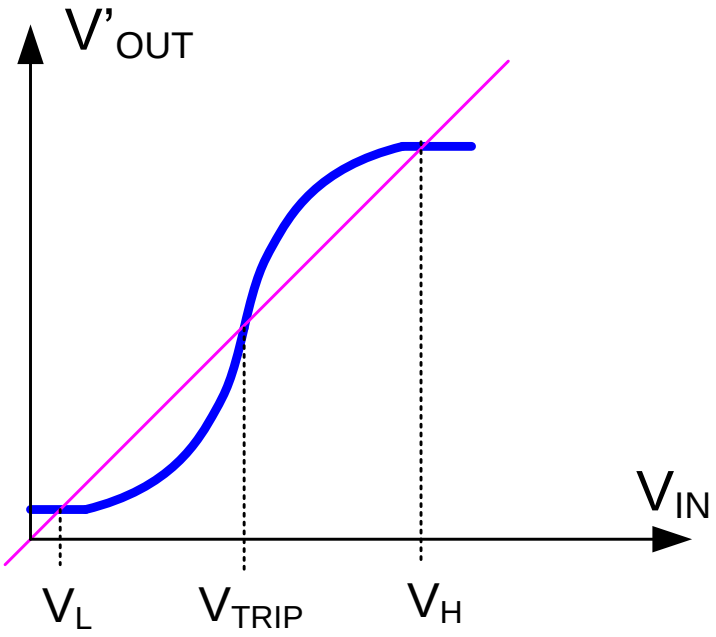


V_H and V_L often termed the “1” and “0” states

Ask the inverter how it will interpret logic levels



Inverter pair



When $V'_{OUT}=V_{IN}$, V_H and V_L are stable operating points, V_{TRIP} is a quasi-stable operating point

Observe: slope of IPTC is greater than 1 at V_{TRIP} and less than 1 at V_H and V_L

Stay Safe and Stay Healthy !

End of Lecture 36

What Characteristics of a Logic Family are Desirable?

Student List:

- Speed
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- (
- S
- |
- (ility)
- Well Defined Logic Levels

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